DESIGN OF AREA-EFFICIENT AND HIGHLY RELIABLE RHBD 10T MEMORY CELL FOR AEROSPACE APPLICATIONS

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ABSTRACT
In this project, based on upset physical mechanism together with reasonable transistor size, a robust 10T memory cell is first proposed to enhance the reliability level in aerospace radiation environment, while keeping the main advantages of small area, low power, and high stability. Using the TANNER EDA tool, simulations performed demonstrate the ability of the proposed radiation-hardened-by-design 10T cell to tolerate both 0 _ 1 and 1 _ 0 single node upsets, with the increased read/write access time. However, when considering the constraints of the target applications, compared with other hardened memory cells, the proposed RHBD 10T cell can be regarded as a good choice for aerospace applications as it provides a good balance among performance, area, power, and reliability for memories working at radiation environment.

INTRODUCTION

MEMORIES are extensively used in aerospace applications as the medium to store data in which single event upsets (SEUs) induced by radiation particles are becoming one of the most significant issues. Because they can conduce to the data corruption in a memory chip and the circuit itself is not permanently damaged, SEUs are also described as the soft errors. Therefore, SEUs can cause a malfunctioning of an electronic system. In some critical memory applications (e.g., satellite equipment and cardioverter defibrillators, SEUs can be detrimental and crucial.

However, radiation hardening techniques for memories are one of the bottlenecks in providing fault tolerance. For many years, some radiation-hardening-by-design (RHBD) techniques have been used to tolerate soft errors in memories using standard commercial CMOS foundry processes, with no modifications to the existing process or violation of design rules.

SRAM-based field-programmable gate arrays (FPGAs) have been widely used during the last decades. However, the volatility of SRAM has limited FPGAs in applications where high security and instant power-on are required. The problem can be solved by introducing non-volatile memory (NVM) as the configuration bit. However, the traditional NVM devices, such as antifuse, E2PROM, and flash, require high-voltage process and have poor logic compatibility, thus limiting the logic density and increasing the integration cost of FPGAs.

Emerging NVMs, such as MRAM, PRAM, and RRAM, have been verified with better scalability and logic compatibility. Based on the logic-in-memory concept, lookup table, which is the core building block in FPGAs, has been proposed with non-volatility. First, various non-volatile SRAM (nvSRAM) structures with MRAM and RRAM were proposed to directly replace SRAM in the traditional lookup table to acquire non volatility. However, the size of nvSRAM cell is remarkably larger than that of SRAM, and the write disturbance is also difficult to avoid for half-select RRAM cells. The proposed a two-input non-volatile lookup table (nvLUT) based on MRAM in the current-mode. The six-input nvLUT with serial/parallel magnetic junctions to acquire enough sensing margin logic for low power. The proposed another RAM-based nvLUT for run-time reconfiguration.

Proposed a third type of MRAM-based nvLUT named hybrid-LUT2.However, the ROFF/RON of MRAM is smaller compared with PRAM or RRAM, resulting in less sense margin or larger area due to serial/parallel magnetic junctions. Moreover, the first three MRAM nvLUTs have a mismatch in parasitic *RC* between the selected path in the multiplexer and the reference path, which may cause nvLUT to fail. For hybrid-LUT2, the configuration of MRAM cells shares the same decoding circuit with logic operation, whose inputs may be wired to other logic blocks and cannot be used as the address inputs during configuration. For RRAM. The proposed an nvLUT based on nanobridge. However, the programming path of nanobridge shares the same multiplexer with the logic path for selection, making the size of transistors in the multiplexer considerably large to satisfy the reset voltage for *R*ON. Chen.

Proposed another RRAM-based nvLUT using crossbar array. However, the sneaking paths inherent in crossbar array bring considerable leakage and poor sensing margin of only 10 mV. To sum up, none of the previous work has achieved high reliability against memory and logic variations, low power, high-area efficiency, and low leakage at the same time. This brief introduces a low-power variation-tolerant nvLUT circuit to overcome the issues in the previous work. Because of its large *R*OFF/*R*ON, 1T1R RRAM cell is used as a configuration bit and a reference resistor to provide sufficient sense margin against memory and logic variations.

Thus, the area cost is decreased because no parallel or serial memory cell combinations are needed to guarantee the sense margin. To reduce the power and area, single-stage sense amplifier with voltage clamp (SSAVC) is employed without compromising the reliability. Moreover, matched reference path (MRP) is devised to minimize the parasitic *RC* mismatch between the selected path in the multiplexer and the reference path for reliable sensing against logic variations. Finally, detailed evaluation is carried out to verify the benefits.

LITERATURE SURVEY

"Area and Energy-Efficient Complementary Dual-Modular Redundancy Dynamic Memory for Space Applications" By Robert Giterman, Lior Atias, and Adam Teman (2017)

The limited size and power budgets of space-bound systems often contradict the requirements for reliable circuit operation within high-radiation environments. In this paper, we propose the smallest solution for soft-error tolerant embedded memory yet to be presented. The proposed complementary dual-modular redundancy (CDMR) memory is based on a four-transistor dynamic memory core that internally stores complementary data values to provide an inherent per-bit error detection capability. The proposed memory was implemented in a 65-nm CMOS technology, displaying as much as a 3.5× smaller silicon footprint than other radiation-hardened bit cells. In addition, the CDMR memory consumes less standby power than other considered solutions across the entire operating region.

"Design of Defect and Fault-Tolerant Non-volatile Spintronic Flip-Flops" by Rajendra Bishnoi, Fabian Oboril, and Mehdi B. Tahoori, Senior Member, IEEE (2017)

With technology down scaling, static power has become one of the biggest challenges in a system on chip. Normally off computing using non-volatile (NV) sequential elements is a promising solution to address this challenge. Recently, many NV shadow flip-flop architectures have been introduced in which magnetic tunnel junction (MTJ) cells are employed as backup storing elements. Therefore, without effective defect and fault tolerance for NV flip-flops, the manufacturing yield will be affected severely. In this paper, we propose a fault-tolerant NV latch (FTNV-L) design, in which several MTJ cells are arranged in such a way that it is resilient to various MTJ faults. The simulation results show that our proposed FTNV-L can effectively tolerate all single MTJ faults with a considerably lower overhead than traditional approaches.

"Novel Radiation-Hardened-by-Design (RHBD) 12T Memory Cell for Aerospace Applications in Nanoscale CMOS Technology" by Jing Guo, Lei Zhu, Wenyi Liu, Hai Huang, Shanshan Liu, Tianqi Wang (2017)

In this paper, a novel radiation-hardened-by-design (RHBD) 12T memory cell is proposed to tolerate single node upset and multiple-node upset based on upset physical mechanism behind soft errors together with reasonable layout-topology. The verification results obtained confirm that the proposed 12T cell can provide good radiation robustness. Compared with 13T cell, the increased area, power, read/write access time overheads of the proposed 12T cell respectively. Moreover, its hold static noise which is higher than that of 13T cell. This means that the proposed 12T cell also has higher stability when it provides fault tolerance capability.

"A Highly Reliable Memory Cell Design Combined With Layout-Level Approach to Tolerant Single-Event Upsets " by Chunhua Qi, Liyi Xiao, Member, IEEE, Tianqi Wang, Jie Li, and Linzhe Li (2016)

In this paper, a highly reliable radiation hardened by design memory cell (RHD12) using 12 transistors in a 65-nm CMOS commercial technology is proposed. Combining with layout-level design, the TCAD mixed-mode simulation results indicate that the RHD12 not only can fully tolerant the single-event upset occurring on any one of its single nodes but can also tolerant single-event multiple-node upsets in a single memory cell, which are caused by charge sharing. Moreover, a set of HSPICE post simulations are done to evaluate the RHD12 and other state-of-theart memory cells, which show that our proposed memory cell has better performance, considering the area, power consumption, and access time.

"A Soft Error Tolerant 10T SRAM Bit-Cell With Differential Read Capability " by Shah M. Jahinuzzaman, Member, IEEE, David J. Rennie, Member, IEEE, and Manoj Sachdev, Senior Member, IEEE (2012)

We propose a quad-node ten transistor (10T) soft error robust SRAM cell that offers differential read operation for robust sensing. The cell exhibits larger noise margin in sub-0.45 V regime and less leakage current than the traditional soft error tolerant 12T DICE SRAM cell. When compared to a conventional 6T SRAM cell, the proposed cell offers similar noise margin as the 6T cell at half the supply voltage, thus significantly saving the leakage power. In addition, the cell exhibits lower soft error rate than the 6T cell in accelerated neutron radiation tests carried out at TRIUMF on a 32-kb SRAM implemented in 90-nm CMOS technology.

EXISTING SYSTEM

RHBD 12T MEMORY CELL DESIGN

A. Cell Schematic and Write/Read Timing

RHBD 12T memory cell is shown in Fig. 1. Here, two access transistors, pMOS transistors P5 and P6, have been connected bit-lines BLN and BL to the output nodes QN and *Q*, respectively. Their ON/OFF state is determined by a word-lineWL. It should be noted that when a radiation particle strikes pMOS transistor, only a positive transient pulse (0→1 or 1 → 1 transient pulse) can be generated; on the contrary, only a negative transient pulse (1 → 0 or 0→0 transient pulse) can be induced when a radiation particle strikes Nmos transistor [2]. Therefore, in order to avoid a negative transient Fig. 2. Transient simulation result of the proposed RHBD 12T cell. pulse induced by a radiation particle in Q and QN nodes, pMOS transistors (i.e., transistors P6 and P5) are used as access transistors. Considering the stored 1 state (i.e., QN = 0, *Q* = 1, *S*0 = 0, and *S*1 = 1) for the proposed RHBD 12T cell (see Fig. 1).

1) When word-line WL is high state 1, transistors P1, P4, P7, N2, and N3 are ON, and the remaining transistors are OFF. Thus, nodes Q and QN are not changed, and they also stored their original data, respectively.

2) Before read operation is executed in the proposed 12T memory cell, two bit-lines BL and BLN need to be precharged to supply voltage VDD. After read operation, and word-lineWL is 0 state, the output node *Q* will store its original state 1 without changing. However, because transistors P5, P7, and N2 are ON, bitline BLN will be discharged. Next, when the voltage difference between two bit-lines BL and BLN are obtained, the differential sense amplifier in memories will output the stored data.

3) To write data 0 into the proposed 12T cell, word-lineWL and bitline BL need to be 0 state, and bitline BLN must be 1 state. Subsequently, node Q will be pulled down to 0 state, and node QN will be pulled up to 1 state. Transistors P2, P3, P8, N1, and N4 will be ON, and transistors P1, P4, P7, N2, and N3 will be OFF. When word-line WL is pulled back to high state 1, the stored data will be 0. This means that data 0 can be successfully written into the proposed RHBD 12T memory cell. Fig. 2 shows a "write 0, read 0, write 1, and read 1" transient simulation result. From Fig. 2, we can see that the proposed cell can rightly achieve write and read operations.

B. SEU Recovery Analysis

In this section, the SEU recovery analysis results for the proposed RHBD 12T memory cell are presented. Considering the state shown in Fig. 1, node *Q* is not a sensitive node, because it is connected with the drain area of OFF pMOS transistors P6 and P8, and its stored value is 1 state. Therefore, according to the upset physical mechanism, when node Q is strike, only a positive pulse is induced, i.e., node Q will be affected by a 1 → 1 transient pulse so that the stored value of node *Q* is not changed.

1) When node QN is upset by a radiation particle, node QN will be pulled up to state 1, then transistors P1 and P4 will be OFF. Subsequently, nodes *Q* and S1 will remain the original logic 1 state without losing voltage value. Therefore, transistor N3 will not be OFF, and node S0 keeps its original 0 state. Transistor P7 and N2 will be ON state, and then, node QN will be pulled back to its original state 0.

2) When a radiation particle strikes node S0, its value will be changed. Then, transistor P7 is temporarily turned OFF, and transistor N1 is temporarily turned ON, and thus, node S1 will be pulled down to 0. However, because of capacitive effect, node QN will not be changed to 1 state, and transistors N4 and P1 keep their OFF and ON states, respectively. Therefore, node Q will be unchanged through ON transistor P4, and node S1 can recover to initial 1 state. Finally, transistor N3 are turned ON, and node S0 will be pulled back to its original 0 state.

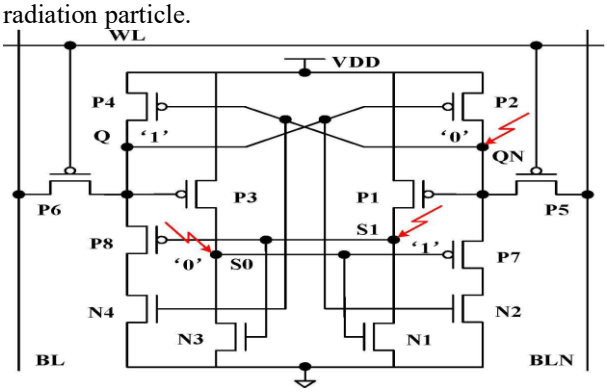
3) When the state of node S1 is changed to 0 from original 1 state by a radiation particle, transistors N3 and P8 will be turned OFF and ON, respectively. Because the voltages of nodes Q, QN, and S0 will be unchanged, transistor P1 remains ON. Therefore, node S1 will be pulled back to its original 1 state through ON transistor P1.

4) When a radiation particle strikes a semiconductor device because of charge sharing effect, multiple sensitive nodes may be affected. In the proposed 12T memory cell, if node pair S0–S1 is upset, transistors P7 and P8 will be temporarily turned OFF and ON, respectively. Subsequently, the analysis is the same as the analysis when the stored value of node S0 is changed. Therefore, nodes S0 and S1 will be pulled back to the original state, respectively.

5) Due to charge sharing effect, the voltage of node pair S0–QN or S1–QN can be changed, the stored state of the proposed 12T cell will be changed. Because both transistors P8 and N4 will be ON, and thus, node *Q* will be pulled down to state 0. This case is similar to a write 0 operation.

Therefore, when node S0 or S1 or QN or node pair S0–S1 in the proposed RHBD 12T cell is upset by a radiation particle, the stored data can be recovered from a corrupted data. When node pair S0–QN or S1–QN is upset, the stored data cannot be recovered. However, when the spacing of node QN and node pair S0–S1 is large enough, the possibilities of the multiple-node upset

cases can be minimized. Fig. 3 shows the layout of the proposed 12T memory cell in which the transistors–transistor spacing's of both node pairs S1–QN and S0–QN is greater than the effective range of charge sharing (about 1.5 μm) Therefore, in this paper, we focus only on the case when node pair S0–S1 is changed by a radiation particle.



RHBD 12T memory cell.

PROPOSED HARDENED 10T MEMORY DESIGN

A. Schematic and Normal Operation Analysis

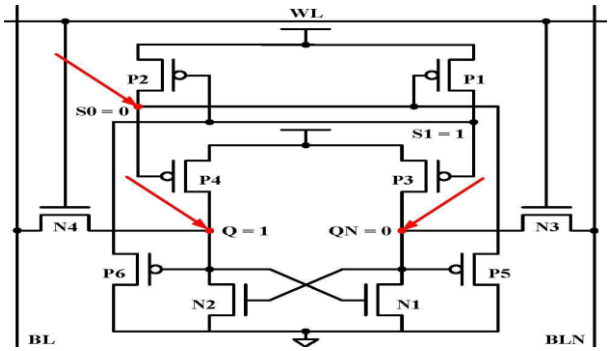


Fig. 2. Schematic of the proposed RHBD 10T memory cell.

For the proposed RHBD 10T memory cell, Fig.2 describes its basic schematic structure. From this figure, it can be seen that the proposed RHBD memory cell consists of ten transistors in which PMOS transistors are transistors P1 _ P6, and the remaining transistors (N1 _ N4) are NMOS transistors. Both NMOS transistors N4 and N3 are defined as the access transistors, and their gates are connected with a word line (WL). Hence, when this WL is in high mode (WL = 1), two access transistors are turned ON. At the moment, write/read operation can be implemented. The stored nodes are nodes Q, QN, S1, and S0 in which these four nodes are responsible for keeping the stored value correctly. In order to quickly transmit the digital signal to the output port during a read operation, a differential sense amplifier has to be employed and connected with two bit lines BL and BLN. Assuming that the stored value of the proposed RHBD 10T memory cell is 1 in digital logic, i.e., $Q = 1$, QN = 0, $S1 = 1$, and $S0 = 0$, as shown in Fig. 1. It is easily concluded that the proposed RHBD 10T memory cell is steadily maintaining the stored value when WL is driven by a low voltage (WL = 0). Before normal read operation, due to precharge circuitry, the voltages of the bit lines BL and BLN will be raised to 1 in digital logic.

In read operation, WL is in high mode (WL = 1), and then two access transistors N3 and N4 are turned ON immediately. Nodes Q, QN, S1, and S0 are keeping the stored value, and the voltage of bit line BL is also unchanged. However, the voltage of bit line BLN is decreased due to the discharge operation through ON transistors N1 and N3. Once the voltage difference of bit lines is a constant value which has been confirmed in the differential sense amplifier connecting with two bitlines, the stored digital signal in memory cell will be output as soon as possible.

The purpose of write operation is to change the stored logical value correctly. Therefore, before write operation, due to the write circuitry, the voltages of bitline BL will be 0 in digital logic. Contrary to the voltage of bitline BL, the voltage of bitline BLN will be 1. When the voltage of WL is supply voltage VDD (WL = 1), write operation is executed. Transistors N2, P2, P3, and P6 are turned ON. At the moment, the states of transistors N1, P1, P4, and P5 will be OFF, so that the logical value of this memory cell is rightly changed to 0. Therefore, write operation can also be completed successfully.

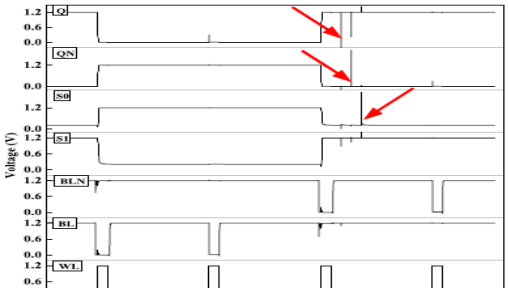


Fig 3. Timing and SEU simulation verification.

Fig.3 Timing and SEU simulation verification. The timing simulation of the proposed RHBD 10T cell has been obtained in Cadence Spectre with models derived from Taiwan Semiconductor Manufacturing Company (TSMC) CMOS 65-nm technology, as shown in Fig. 2. From this figure, we can see that a "write 0, read 0, write 1, and read 1" timing simulation result is successfully completed. Therefore, the proposed RHBD 10T memory cell can rightly achieve its timing operation.

B. SEU Recovery Analysis

Let us consider the stored 1 state again, as shown in Fig. 1. For the RHBD 10T memory cell, according to SEU

physical mechanism, nodes Q, QN, and S0 are three sensitive nodes for this stored value.

1) If the sensitive node Q is flipped to state 0 by a charged particle, transistor N1 will be temporarily OFF, and the switch state of transistor P6 will be ON temporarily. However, the voltage of node S1 will be its initial state, because the size of transistor P1 is larger than that of transistor P6 (2.1× larger). As a result, the voltage of node S0 is unchanged. Hence, transistor P4 will be always ON. Finally, the voltage of node Q will be flipped to the initial voltage.

2) If the sensitive node S0 is induced to change the initial state by a radiation particle, both transistors P1 and P4 will be temporarily turned OFF, and the nodes Q, QN, and S1 will be unchanged due to capacitive effect. Therefore, transistor P5 will be always ON, and the voltage of node S0 will be restored.

3) When node QN is flipped, the switch states of transistors N2 and P5 will be temporarily turned ON and OFF, respectively, and then the voltage of node Q will be changed to 0 state.
Hence, transistors P6 and N1 will be also temporarily turned ON and OFF, respectively. However, due to the larger size of transistor P1, the value of node S1 will be its initial value so that transistor P2 also remains its OFF state. Therefore, the affected node Q will be pulled up to 1 state, and then transistor N1 will be turned ON again, and node QN will be pulled down to 0 state.

RHBD (RADIATION HARDENED BY DESIGN):
Radiation hardening is the act of making electronic components and systems resistant to damage or malfunctions caused by ionizing radiation (particle radiation and high-energy electromagnetic radiation), such as those encountered in outer space and high-altitude flight, around nuclear reactors and particle accelerators, or during nuclear accidents or nuclear warfare.
Most semiconductor electronic components are susceptible to radiation damage; radiation-hardened components are based on their non-hardened equivalents, with some design and manufacturing variations that reduce the susceptibility to radiation damage. Due to the extensive development and testing required to produce a radiation-tolerant design of a microelectronic chip, radiation-hardened chips tend to lag behind the most recent developments.
Radiation-hardened products are typically tested to one or more resultant effects tests, including total ionizing dose (TID), enhanced low dose rate effects (ELDRS), neutron and proton displacement damage, and single event effects (SEE, SET, SEL and SEB).

Problems caused by radiation
Radiation damage Environments with high levels of ionizing radiation create special design challenges. A single charged particle can knock thousands of electrons loose, causing electronic noise and signal spikes. In the case of digital circuits, this can cause results which are inaccurate or unintelligible. This is a particularly serious problem in the design of satellites, spacecraft, military aircraft, nuclear power stations, and nuclear weapons. In order to ensure the proper operation of such systems, manufacturers of integrated circuits and sensors intended for the military or aerospace markets employ various methods of radiation hardening. The resulting systems are said to be radiation-hardened, rad-hard, or (within context) hardened.

APPLICATIONS:

- **Digital signal processing**

Digital signal processing (DSP) is the mathematical manipulation of information signal to modify or improve it in some way. It is characterized by the representation of discrete time, discrete frequency, or other discrete domain signals by a sequence of numbers or symbols and the processing of these signals., Sonar and radar signal processing, sensor array processing, spectral estimation, statistical signal Processing, digital image processing, signal processing for communications, control of systems, Biomedical signal processing, seismic data processing, etc.
The goal of DSP is usually to measure, filter, and/or compress continuous real-world analog signals. Digital signal processor (DSP) is a specialized microprocessor with an architecture optimized for the fast operational needs of digital signal processing.

- **Mobile phone**

A mobile phone is a device that can make and receive telephone calls over a radio link whilst moving around a wide geographic area. It does so by connecting to a cellular network provided by a mobile phone operator, allowing access to the public telephone network. In these mobile phones they want to reduce the area as well as the power. So our adder design is used to mobile phones.

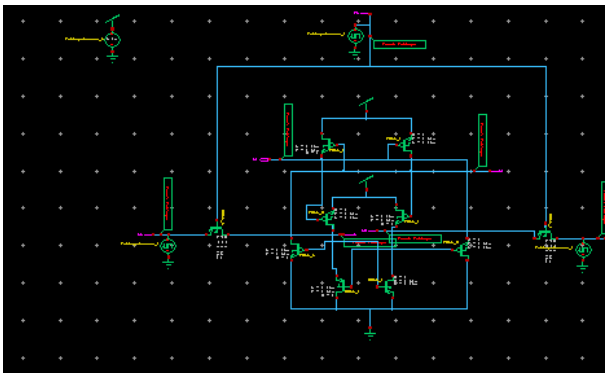
- **Satellite application**

Satellites are used for a large number of purposes. Common types include military and Civilian Earth observation satellites, communications satellites, navigation satellites weather satellites, and research satellites. Space stations and human spacecraft in orbit are also satellites.
Satellite orbits vary greatly, depending on the purpose of the satellite, and are classified in a number of ways. Well-known (overlapping) classes include low Earth orbit, polar orbit, and geostationary orbit. Satellites are usually semi-independent computer-controlled systems. Satellite

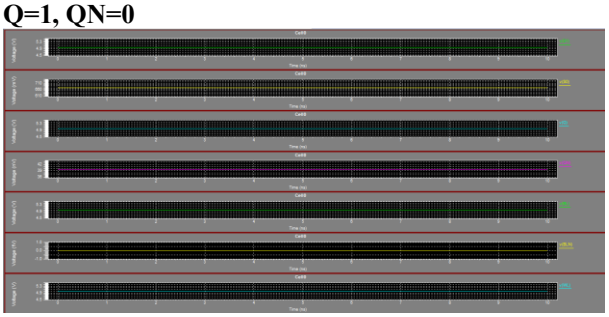
subsystems attend many tasks, such as power generation, thermal control, telemetry, attitude control, and orbit control. In this control unit, our adder will be used for some area efficient products.

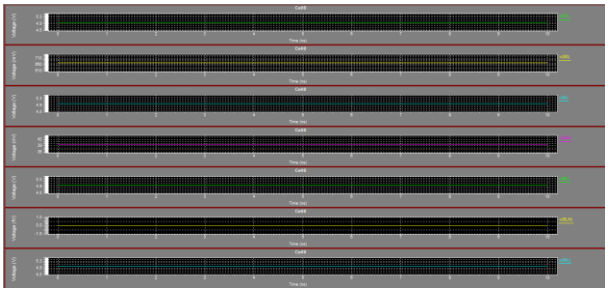
RESULTS AND DISCUSSION

Design implementation in Tanner EDA tool:

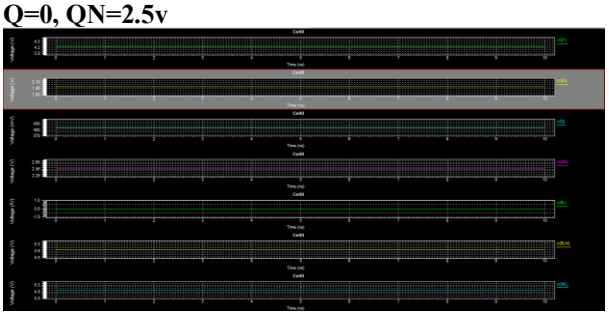


(i) When BL = 1, BLN=0
Q=1, QN=0





(ii) When BL = 0, BLN=1
Q=0, QN=2.5v



TIMING REPORT:

```
Parsing                          0.01 seconds
Setup                            0.01 seconds
DC operating point               0.05 seconds
Transient Analysis               0.00 seconds
Overhead                         0.06 seconds
-----------------------------------------
Total                            0.13 seconds
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POWER ANALYSIS

```
Power Results
Total Power from time 0 to 1e-008
Average power consumed -> 1.460419e-002 watts
Max power 1.460419e-002 at time 0
Min power 1.460419e-002 at time 0
```

CONCLUSION

A novel RHBD 10T cell in TANNER EDA, CMOS process is proposed in this brief. Compared with previous hardened 10T memory cell, the proposed cell can recover an error in any one sensitive node. The simulation results present that the penalty introduced for the proposed 10T cell is the increased write/read access time that may affect its applications with high-speed requirements. However, when considering the constraints of the target applications, compared with other hardened memory cells, the proposed RHBD 10T cell can be regarded as a good choice for aerospace applications as it provides a good balance among performance, area, power, and reliability for memories working at radiation environment.

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